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Dual-T-Type Seven-Level Boost Active-Neutral-Point-Clamped (DTT-7L-BANPC) Inverter

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Abstract: - The conventional three-level active-neutral-point-clamped (ANPC) inverter requires high DC-link voltage at least twice the peak of AC output. To reduce the DC-link voltage, a recent topology that enhanced the voltage gain from half to unity has been presented. In this letter, an alternative ANPC topology is established by using two T-type inverters. Two floating capacitors with self-voltage balancing capability are integrated to achieve a voltage-boosting gain of 1.5. In addition, the proposed topology is capable of generating seven voltage levels. Its operation is validated through circuit analysis followed by experimental results of a prototype.

Index Terms: seven-level, boost ANPC, multilevel inverter, voltage-boosting

I. INTRODUCTION

The three-level active-neutral-point-clamped (ANPC) (3L-ANPC) inverter depicted in Fig. 1(a) is widely used in the industry for DC–AC power conversion [1], [2]. Tremendous research efforts have been devoted to developing ANPC inverters with a higher number of levels [3], but at the expense of the voltage-balancing problem. Additional voltage-balancing circuits with specially designed control algorithms are normally necessary to resolve the balancing problem [4–6].

Improved ANPC topologies that are established by hybrid configuration with other topologies, such as H-bridge and flying capacitor inverters, have also been explored [7], [8]. In [9], an 11-level hybrid topology that consists of a 5L-ANPC and a low-voltage submodule that controls an additional isolated DC-source was presented.

Instead of increasing the number of voltage levels, some studies have attempted to establish different ANPC inverters with switch count reduction, thereby enhancing the efficiency. Following a review of various 5L-ANPC inverter topologies, a novel 5L-ANPC inverter with a more compact configuration was recently demonstrated [10].

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All the above-mentioned ANPC topologies suffer from a common drawback such that they are subjected to a high DC-link voltage requirement. The peak of AC output generated by an ANPC inverter with sinusoidal pulse width modulation (SPWM) is

$$V_{ac,pk} = MI \bullet V_{\max} \quad (1)$$

where MI indicates the modulation index, and $V_{\max}$ indicates the magnitude of the maximum voltage level. Taking the 3L-ANPC inverter shown in Fig. 1(a) as an example, the $V_{\max}$ is 0.5 V_{dc}. In this instance, the DC-link voltage V_{dc} must be at least $2V_{ac,pk}$. In other words, the voltage gain ($V_{\max}/V_{dc}$) of a 3L-ANPC inverter is limited to half. The implications of the restricted gain become particularly apparent in grid-connected renewable energy applications. With the required minimum DC-link voltage V_{dc} twice the AC grid peak voltage, a boost DC–DC converter is essential to generate the demanded DC-link voltage. However, this two-stage power conversion structure reduces the efficiency of the system.

Recently, an innovative ANPC topology has made a single-stage DC–AC power conversion system possible to eliminate the need of a front-end boost DC–DC converter [11]. This ANPC topology is derived based on the principle presented in [12]. It enhances the voltage gain from half to unity, thus reducing the DC-link voltage by half, as shown in Fig. 1(b). It is able to generate five voltage levels from $-V_{dc}$ to V_{dc}.

The initiative of this letter is to propose an alternative ANPC inverter with voltage-boosting capability and with generation of an increased number of levels. The remainder of this letter is organized as follows. In Section II, the proposed ANPC topology is presented. In Section III, the experimental results of a prototype are discussed with simulation results are presented for power losses analysis, and, finally, Section IV is the conclusion.

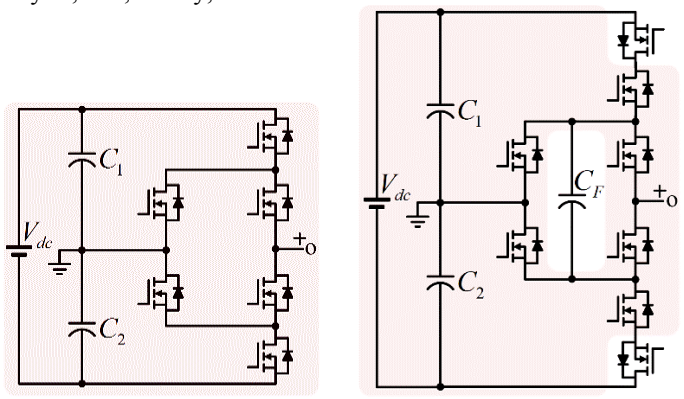

Fig. 1. Active-neutral-point-clamped inverters: (a) conventional three-level ANPC topology and (b) a recent five-level ANPC topology with twofold voltage gain enhancement.

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II. PROPOSED DTT-7L-BANPC INVERTER

The proposed topology is called a "dual-T-type seven-level boost ANPC" (DTT-7L-BANPC) following its circuit structure, which comprises two T-type inverters, as depicted in Fig. 2. Considering that all the power switches are metal-oxide-semiconductor field effect transistors (MOSFETs), the proposed ANPC inverter requires only two additional power switches to those in the previous study [11]. Two floating capacitors (C_{F1} and C_{F2}) are integrated to achieve a voltage-boosting gain of 1.5. With the magnitude of each level is $0.5V_{dc}$, the proposed topology is capable of generating seven levels from $-1.5V_{dc}$ to $1.5V_{dc}$.

Analysis of the proposed DTT-7L-BANPC inverter is illustrated in Fig. 3. The floating capacitor C_{F1} is charged to V_{dc} when S4 and S9 are ON during 0.5 V_{dc} and –1.5 V_{dc}. In contrast, C_{F2} is charged to V_{dc} during 1.5 V_{dc} and –0.5 V_{dc}. The floating capacitors operate symmetrically for each half-cycle, which results in self-balancing of their voltages during operation.

By discharging C_{F1} either through the neutral point or in series with the DC-link capacitor C_1, two additional voltage levels (V_{dc} and 1.5 V_{dc}) to that in the 3L-ANPC and one additional voltage level ($1.5V_{dc}$) to that in the 5L-Boost-ANPC [11] can be achieved during the positive half-cycle. For the negative half-cycle, floating capacitor C_{F2} is used to generate $-V_{dc}$ and -1.5 V_{dc}. This implies the superiority of the proposed DTT-7L-BANPC in attaining enhanced voltage-boosting gain and generation of an increased number of levels. A comparison between the proposed DTT-7L-BANPC and 5L-Boost-ANPC [11] is summarized in Table I.

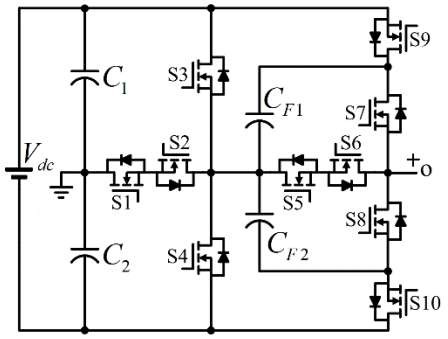

Fig. 2. Proposed DTT-7L-BANPC inverter.

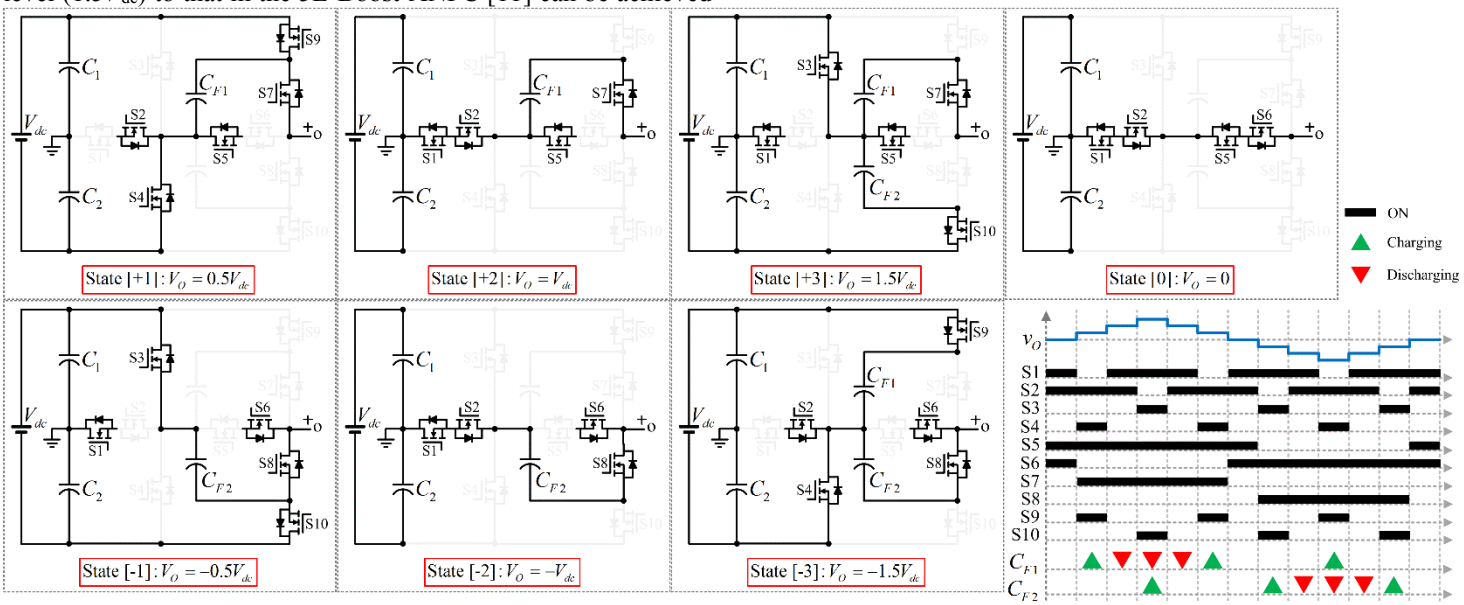

Fig. 3. Analysis of the proposed DTT-7L-BANPC inverter.

TABLE I
COMPARISON BETWEEN THE PROPOSED DTT-7L-BANPC AND TOPOLOGY IN [11]

	Topology in [11] (5L-Boost-ANPC)	Proposed topology (DTT-7L-BANPC)
Number of levels	5	7
Number of switches	8	10
Maximum level, V_{max}	V_{dc}	$1.5V_{dc}$
Voltage gain (V_{max}/V_{dc})	1	1.5
Number of floating capacitors	1	2

Table II and III summarize the blocking voltage and conducting current for each switch in the proposed DTT-7L-BANPC during each voltage level. All the ten switches in the topology can be classified into five pairs such as S1–S2, S3–S4, S5–S6, S7–S8, and S9–S10. The switches in each pair operate symmetrically and experience the same voltage stress and current stress, thus renders equal power losses. It is also apparent that the number of conducting switches for load current is low to reduce conduction losses. The load current flows through four switches for zero level ([0]), three switches for second level ([+2], [-2]) and only two switches for the remaining levels ([+1], [[+3], [-1], [-3]).

TABLE II
VOLTAGE STRESS ON POWER SWITCHES DURING EACH VOLTAGE LEVEL

	[0]	[+1]	[+2]	[+3]	[-1]	[-2]	[-3]
S1	0	$0.5V_{dc}$	0	0	0	0	$0.5V_{dc}$
S2	0	0	0	$0.5V_{dc}$	$0.5V_{dc}$	0	0
S3	$0.5V_{dc}$	V_{dc}	$0.5V_{dc}$	0	0	$0.5V_{dc}$	V_{dc}
S4	$0.5V_{dc}$	0	$0.5V_{dc}$	V_{dc}	V_{dc}	$0.5V_{dc}$	0
S5	0	0	0	0	V_{dc}	V_{dc}	V_{dc}
S6	0	V_{dc}	V_{dc}	V_{dc}	0	0	0
S7	V_{dc}	0	0	0	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$
S8	V_{dc}	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	0	0	0
S9	$0.5V_{dc}$	0	$0.5V_{dc}$	V_{dc}	V_{dc}	$0.5V_{dc}$	0
S10	$0.5V_{dc}$	V_{dc}	$0.5V_{dc}$	0	0	$0.5V_{dc}$	V_{dc}

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TABLE III
CURRENT STRESS ON POWER SWITCHES DURING EACH VOLTAGE LEVEL

	[0]	[+1]	[+2]	[+3]	[-1]	[-2]	[-3]
S1	I_{Load}	0	I_{Load}	0	0	I_{Load}	0
S2	I_{Load}	0	I_{Load}	0	0	I_{Load}	0
S3	0	0	0	I_{Load} $+I_{charge}$	I_{charge}	0	0
S4	0	I_{charge}	0	0	0	0	I_{Load} $+I_{charge}$
S5	I_{Load}	0	0	0	0	0	0
S6	I_{Load}	0	0	0	0	0	0
S7	0	I_{Load}	I_{Load}	I_{Load}	0	0	0
S8	0	0	0	0	I_{Load}	I_{Load}	I_{Load}
S9	0	I_{Load} $+I_{charge}$	0	0	0	0	I_{charge}
S10	0	0	0	I_{charge}	I_{Load} $+I_{charge}$	0	0

I_{Load} is the load current, and I_{charge} is the floating capacitors charging current.

III. SIMULATION AND EXPERIMENTAL RESULTS

To validate the operation of the proposed DTT-7L-BANPC inverter, an experimental prototype, as shown in Fig. 4, was implemented. Experimental tests were conducted with an input voltage V_{dc} of 100V and a series resistor–inductor load of 40Ω and 0.1H. The prototype specifications are summarized in Table IV.

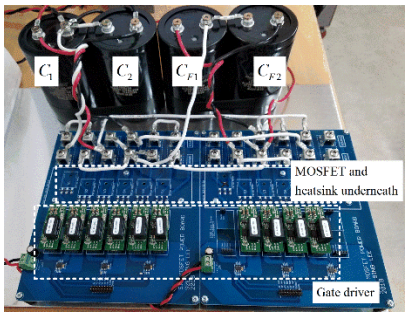

Fig. 4. Experimental prototype of the proposed DTT-7L-BANPC inverter

TABLE IV
PROTOTYPE SPECIFICATIONS

Description	Value/Parameter
Input voltage, V_{dc}	100 V
Carrier frequency	5kHz
Load resistor	40 Ω
Load inductor	0.1 H
Capacitor, C_1, C_2, C_{F1}, C_{F2}	ALS30A472NJ450
Power switch	C3M0120090D

The precomputed switching angles using selective harmonic elimination pulse width modulation (SHEPWM) were first considered to analyze the operation of the proposed topology. Fig. 5 shows that the average floating capacitor voltages is equal to the input voltage V_{dc} of 100V. Seven distinct voltage levels with the magnitude of each level equal to 50V were clearly observed. The voltage ripples of the floating capacitors were also measured. It is apparent from Fig. 5 that C_{F1} was charged during 50V and –150V, discharged during 100V and 150V, and constant elsewhere. Symmetrical operation for C_{F2} was observed such that it was charged during 150V and –50V and discharged during –100V and –150V. Good agreement between the experimental results and analysis conducted in Fig. 3 has validated the operation of the proposed DTT-7L-BANPC inverter.

Experiments were proceeded to test the proposed DTT-7L-BANPC topology with SPWM. SPWM signals generated by a modulator shown in Fig. 6 was implemented in a FPGA controller. Fig. 7 shows the measured waveforms at a modulation index (MI) of 1.0. The waveforms once again validated the performance of the proposed topology in achieving a voltage gain of 1.5 with generation of seven voltage levels.

Fig. 8 shows the transient response of the proposed DTT-7L-BANPC inverter for a load step from no load to full load. The load current increases instantly when the load is turned ON, without influencing the performance of the output voltages and the average floating capacitor voltages.

Experiments with SPWM were repeated at different MIs. The input and output power were measured to determine the efficiency of the experimental prototype. It is evident from Fig. 9 that the proposed DTT-7L-BANPC inverter is highly efficient, with the peak efficiency recorded at 98.3%. Fig. 9 also shows that the measured root mean square of the output voltage at an MI of 1.0 was 107V, which indicates a peak magnitude of approximately 151V. The peak of AC output voltage is 1.5 times that of the input voltage, thereby validating the voltage-boosting capability of the proposed topology.

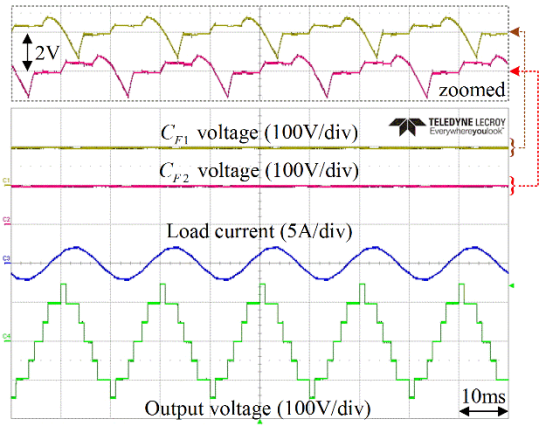

Fig. 5. Measured waveforms with precomputed switching angles with SHEPWM.

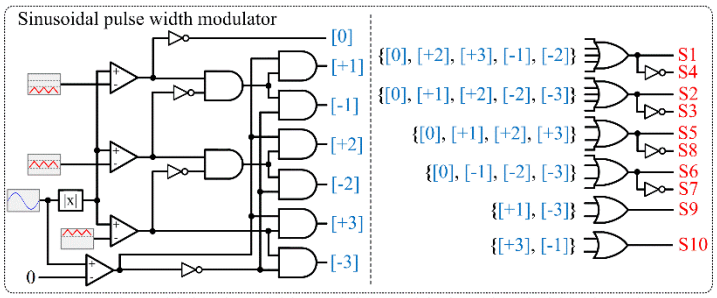

Fig. 6. Sinusoidal pulse width modulator with three level-shifted carriers.

To further validate the efficiency of the proposed DTT-7L-BANPC, the power switches used in the prototype were modelled in PSIM software according to the specifications listed on datasheet. Simulation was first conducted considering the experimental prototype parameters at MI of 1.0. The power losses analysis summarized in Table V indicates that the simulated efficiency was approximately 98.2%. Simulation was then conducted to consider higher output power generation in a grid connected application,

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where the AC grid peak voltage is 330V. The input voltage was set to 220V which is 2/3 of the AC grid peak voltage. The simulated efficiency was approximately 97.4%, with an output power of 1333.8W. It is also evident from the simulation that the proposed DTT-7L-BANPC inverter is endowed with voltage-boosting capability with $V_{ac,pk} = MI*1.5V_{dc}$.

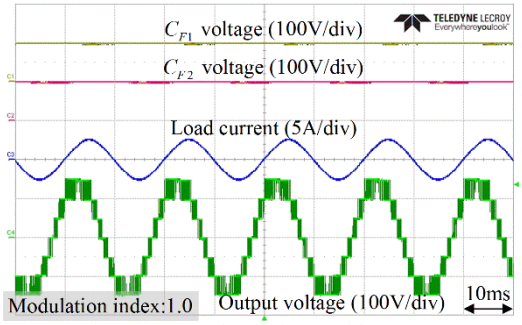

Fig. 7. Measured waveforms with SPWM.

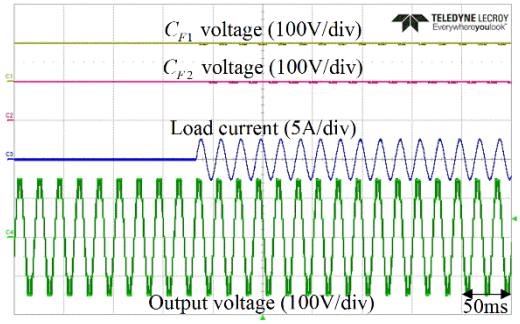

Fig. 8. Measured waveforms during load transient.

TABLE V
POWER LOSSES ANALYSIS USING PSIM SOFTWARE

	(a)	(b)
RMS output voltage (V)	107	231
Losses of S1 (W)	0.18	1.06
Losses of S2 (W)	0.18	1.06
Losses of S3 (W)	0.42	8.05
Losses of S4 (W)	0.42	8.05
Losses of S5 (W)	0.04	0
Losses of S6 (W)	0.04	0
Losses of S7 (W)	0.2	2
Losses of S8 (W)	0.2	2
Losses of S9 (W)	0.5	6.5
Losses of S10 (W)	0.5	6.5
Total losses (W)	2.68	35.22
Output power (W)	150	1333.8
Efficiency (%)	98.2	97.4

(a): Using experimental parameters at MI of 1.0
(b): V_{dc} was increased to 220V (to produce a peak voltage of 330V – considering AC grid voltage) with purely resistive load

IV. CONCLUSION

A novel inverter topology, DTT-7L-BANPC, is reported in this letter. As the name implies, the proposed topology is capable of generating seven voltage levels with a voltage-boosting gain of 1.5. Self-voltage balancing of two floating capacitors was achieved during operation. The proposed topology was analyzed and tested. Experimental results validated its operation and feasibility. It is an alternative for a single-stage multilevel boost DC–AC power conversion system.

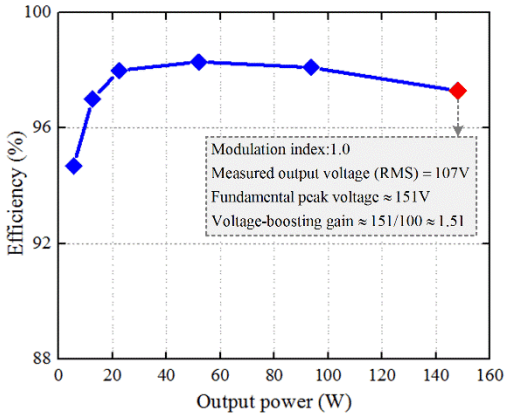

Fig. 9. Efficiency of the experimental prototype.

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